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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,619	07/26/2001	Chih Hsin Wang	2102397-910600	4762

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EXAMINER	
BERRY, RENEE R	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/916,619	Applicant(s) Wang
	Examiner Renee Berry	Art Unit 2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-88* is/are pending in the application.

4a) Of the above, claim(s) *1-40 and 45-84* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *41-44 and 85-88* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group II in Paper No. 9 is acknowledged.

2. Claims 1-40 and 45-84 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse in Paper No. 9.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 41-44 and 85-88 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by US patent no. 6,157,575 to Choi.

In regard to claim 41, Choi teaches an electrically programmable and eraseable memory device having a substrate of semiconductor material of a first conductivity type; first and second spaced-apart terminals in the substrate of a second conductivity type with a channel region therebetween; a first insulation layer disposed over the substrate; an electrically conductive floating gate disposed over a first insulation layer and extending over a portion of the channel

region and over a portion of the second terminal; a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and an electrically conductive control gate having a first portion and a second portion, the first portion being substantially rectangularly shaped and positioned immediately adjacent to the second insulation layer, the second portion being substantially a spacer connected to the first portion and disposed over the floating gate and insulated therefrom at column 7, lines 2-39.

In regard to claims 42, 44, 86 and 88, Choi teaches the control gate forms a notch at the connection between the first portion and the second portion at column 9, lines 32-41.

In regard to claim 43, Choi teaches an array of electrically programmable and erasable memory devices having a substrate of semiconductor material of a first conductivity type; spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; each of the active regions including a column of memory cells extending in the first direction, each of the memory cells includes a first and second spaced-apart terminals formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween, a first insulation layer disposed over a substrate including over the channel region, an electrically conductive floating gate disposed over the first insulation layer and extending over a portion of the channel region and over a portion of the second terminal, and a second insulating layer disposed over the adjacent the floating gate and having a thickness permitting Fowler-Nordheim

tunneling of charges therethrough; and a plurality of electrically conductive control gates each extending across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and having a first portion that is substantially rectangular in shape and a second portion that is connected to the first portion and is substantially a spacer, wherein each of the control gates intercepts one of the memory cells in each of the active regions such that the first portion is positioned immediately adjacent to the second insulation layer therein and the second portion is disposed over the floating gate and insulated therefrom at column 7, lines 13-39.

In regard to claim 85, Choi teaches an electrically programmable and eraseable memory device having a substrate of semiconductor material of a first conductivity type; first and second spaced-apart terminals in the substrate of a second conductivity type, with channel region therebetween; a first insulation layer disposed over the substrate; an electrically conductive floating gate disposed over the first insulation layer and extending over a portion of the channel region and over a portion of the second terminal; a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and an electrically conductive control gate having a first portion and a second portion, the first portion having a substantially planar sidewall portion and is positioned immediately adjacent to the second insulation layer, the second portion being substantially a spacer connected to the substantially planar sidewall portion and disposed over the floating gate and insulated therefrom at column 9, lines 8-54.

In regard to claim 87, Choi teaches an array of electrically programmable and eraseable memory devices having a substrate of semiconductor material of a first conductivity type; spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; each of the active regions including a column of memory cells extending in the first direction, each of the memory cells includes a first and second spaced-apart terminals formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween, an electrically conductive floating gate disposed over the first insulation layer and extending over a portion of a channel region and over a portion of the second terminal, and a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and a plurality of electrically conductive control gates each extending across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and having a first portion that has a substantially planar sidewall portion and a second portion that is connected to the substantially planar sidewall portion sidewall portion and is substantially a spacer, wherein each of the control gates intercepts one of the memory cells in each of the active regions such that the first portion is positioned immediately adjacent to the second insulation layer therein and the second portion is disposed over the floating gate and insulation therefrom at column 7, lines 2-39.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US patent no. 5,293,337 to Aritome et al and US patent no. 6,252,799 to Liu et al. disclose electrically programmable and eraseable memory devices.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. R. Berry whose telephone number is (703) 305-4544.

HOAI HO
PRIMARY EXAMINER

RRB

July 23, 2003